1/10

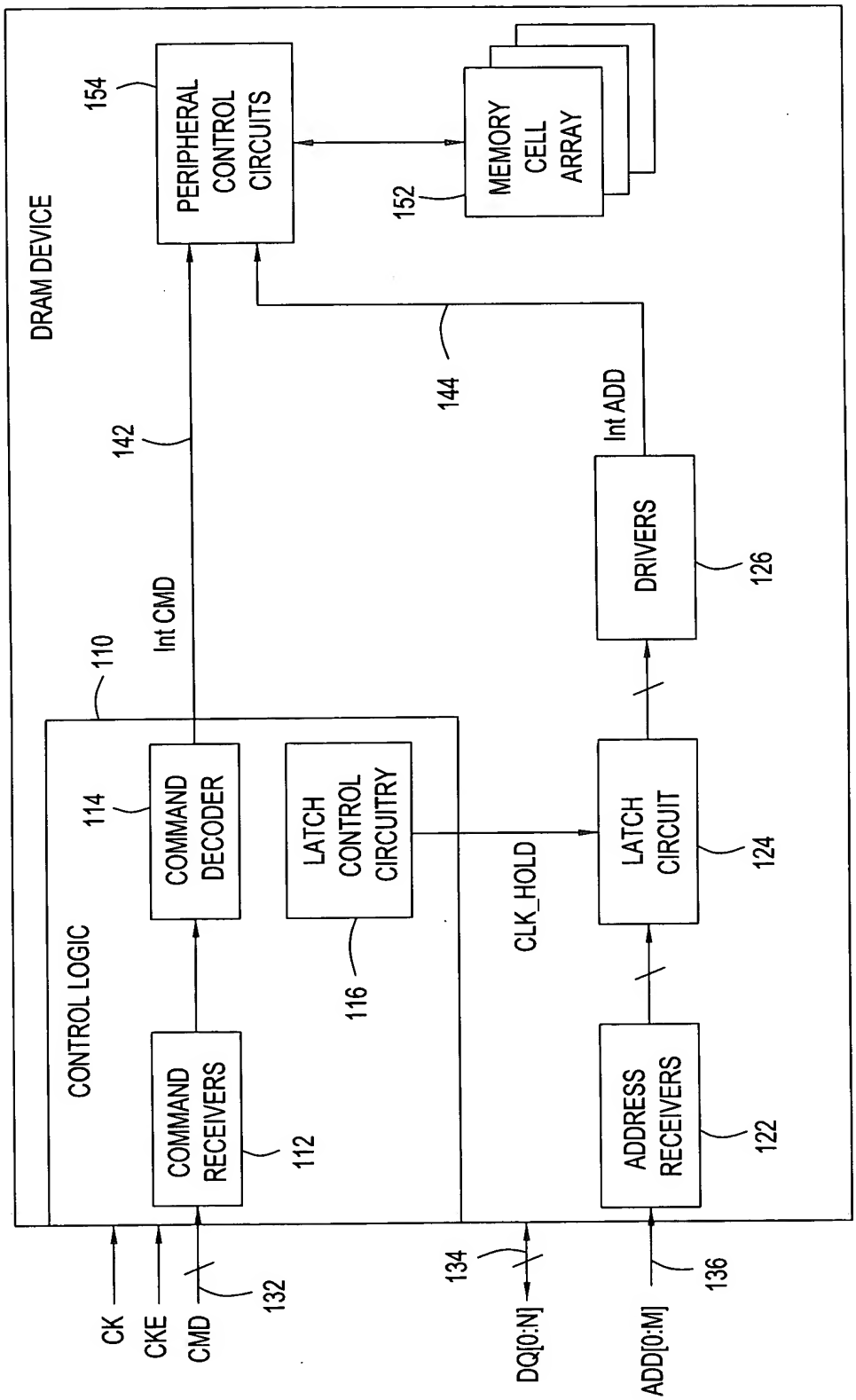
DRAM DEVICE
PERIPHERAL CONTROL CIRCUITS
154
MEMORY CELL ARRAY
152
144
142
Int ADD
DRIVERS
126
Int CMD
110
CONTROL LOGIC
114
COMMAND DECODER
LATCH CONTROL CIRCUITRY
116
CLK_HOLD
LATCH CIRCUIT
124
COMMAND RECEIVERS
112
ADDRESS RECEIVERS
122
CK
CKE
CMD
132
134
136
DQ[0:N]
ADD[0:M]

FIG. 1

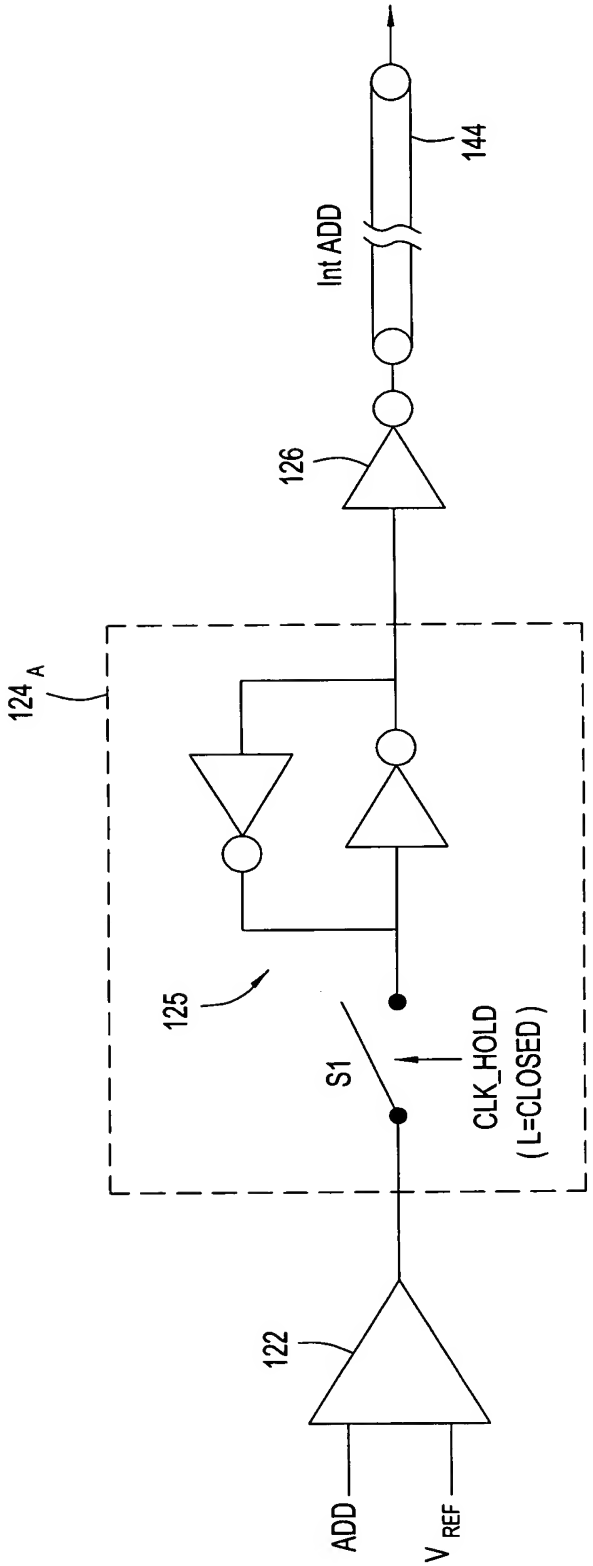

FIG. 2A

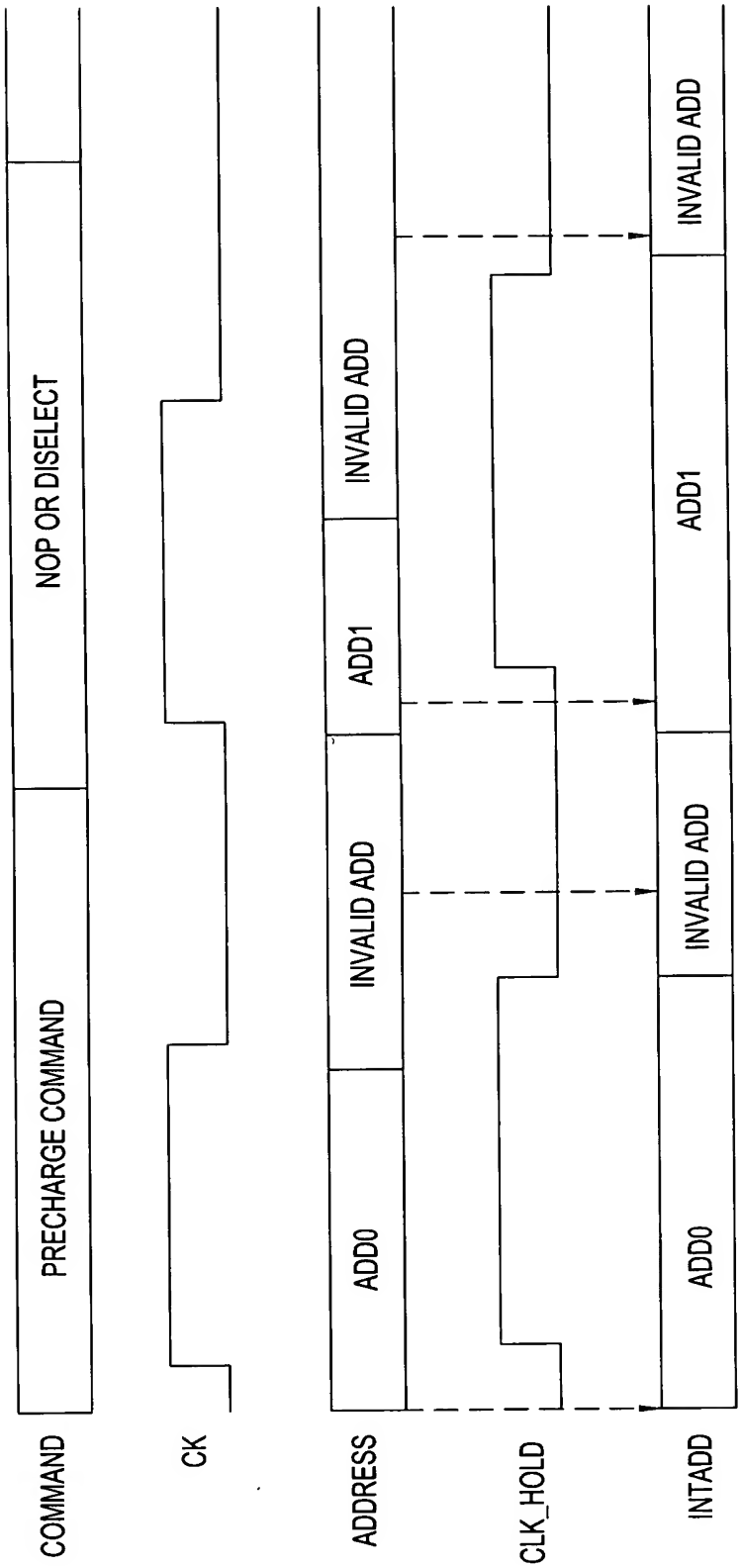
COMMAND
PRECHARGE COMMAND
NOP OR DISELECT
CK
ADDRESS
ADD0
INVALID ADD
ADD1
INVALID ADD
CLK_HOLD
INTADD
ADD0
INVALID ADD
ADD1
INVALID ADD

FIG. 2B

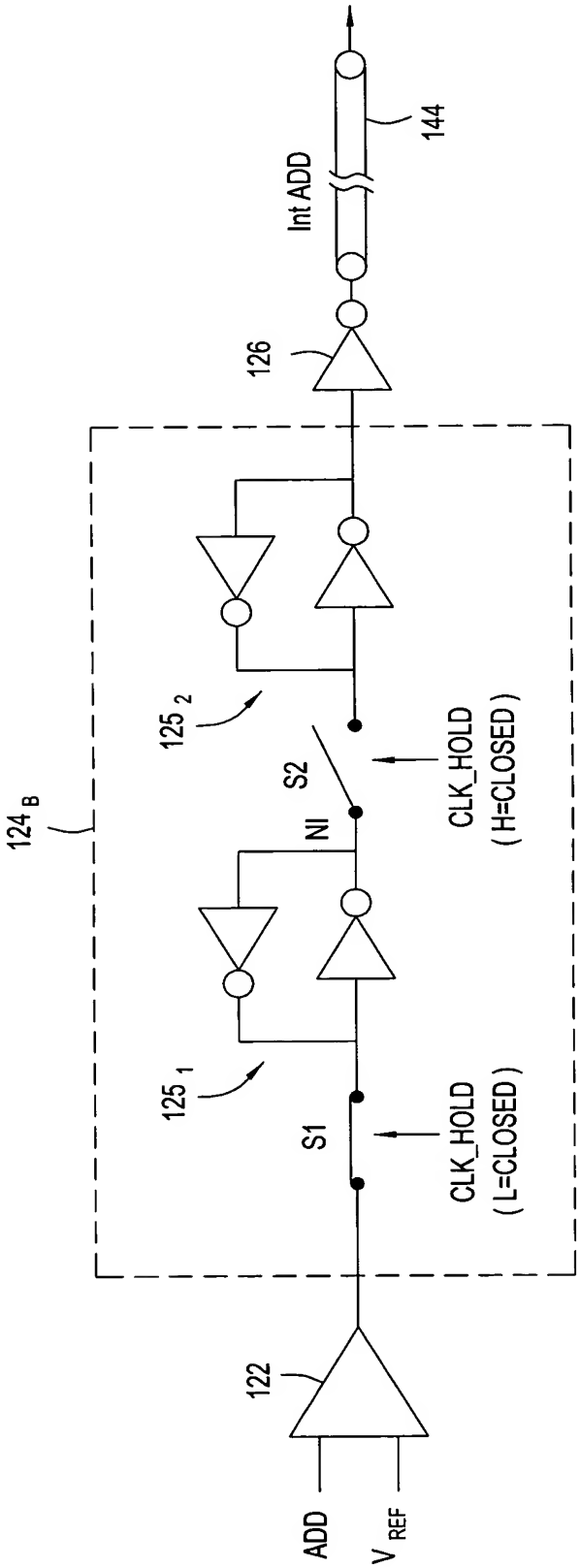

FIG. 3A
(PRIOR ART)

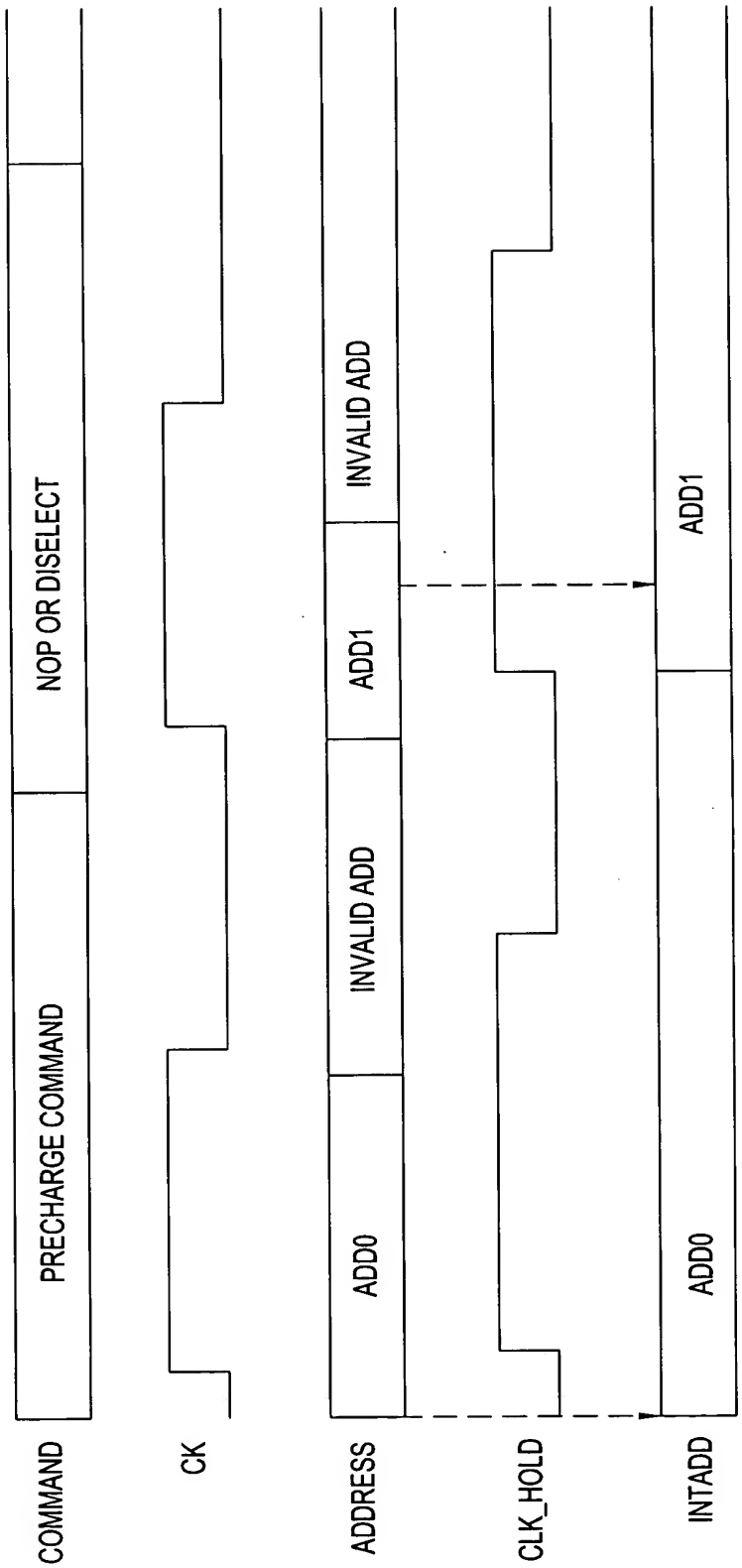

FIG. 3B
(PRIOR ART)

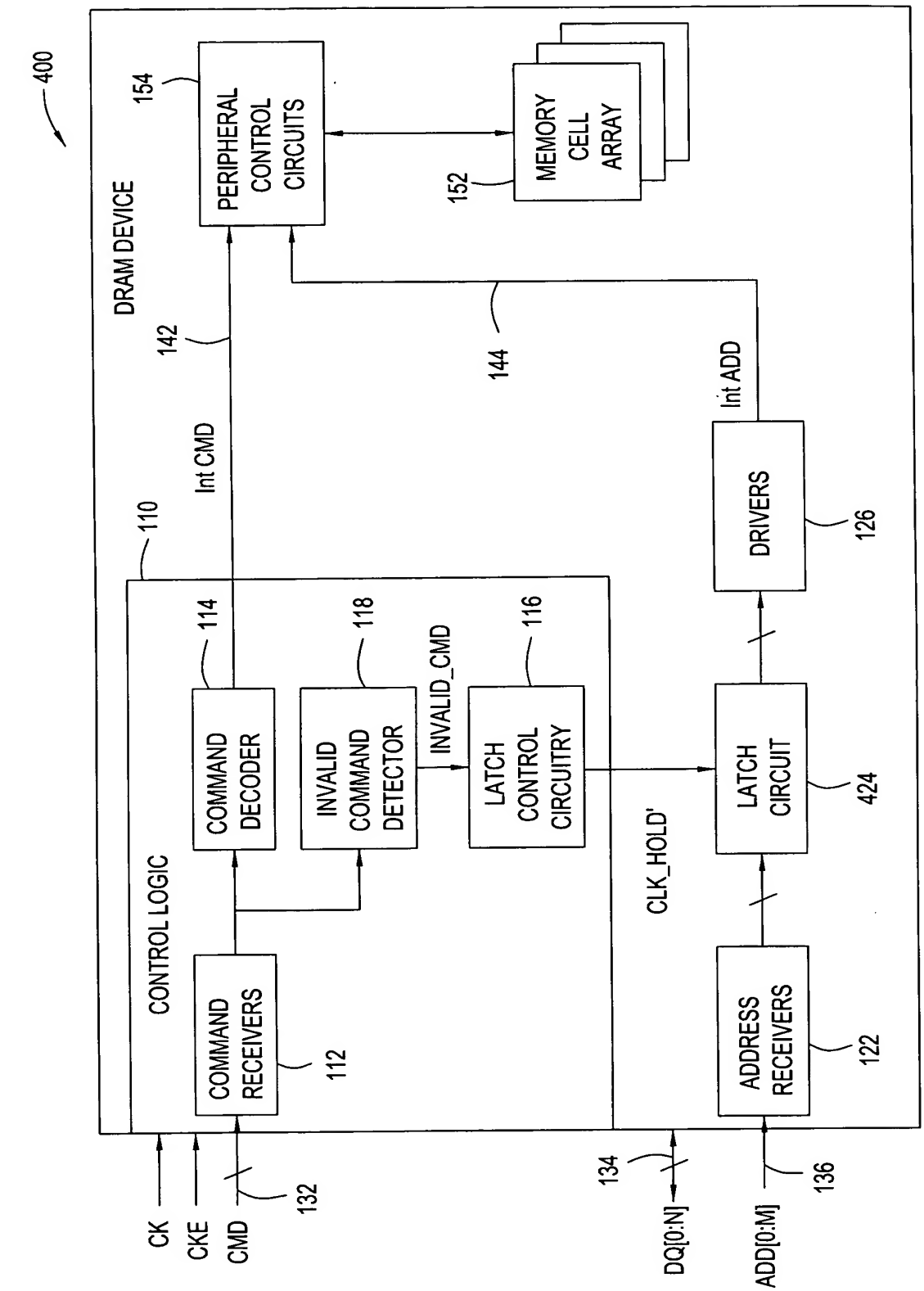
400
DRAM DEVICE
154
PERIPHERAL CONTROL CIRCUITS
152
MEMORY CELL ARRAY
142
144
Int CMD
Int ADD
110
CONTROL LOGIC
114
COMMAND DECODER
118
INVALID COMMAND DETECTOR
INVALID_CMD
116
LATCH CONTROL CIRCUITRY
DRIVERS
126
CLK_HOLD'
LATCH CIRCUIT
424
COMMAND RECEIVERS
112
ADDRESS RECEIVERS
122
CK
CKE
CMD
132
134
136
DQ[0:N]
ADD[0:M]

FIG. 4

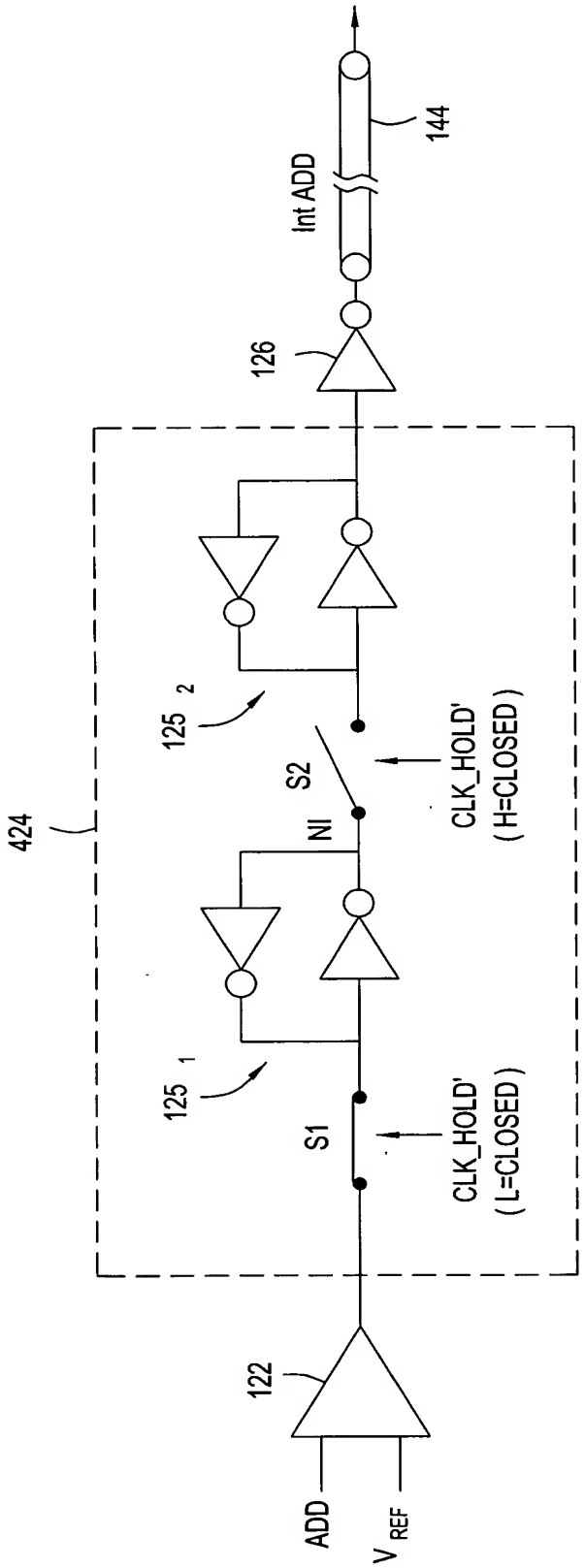
144
Int ADD
126
424
125 2
S2
NI
CLK_HOLD'
(H=CLOSED)
125 1
S1
CLK_HOLD'
(L=CLOSED)
122
ADD
V REF

FIG. 5A

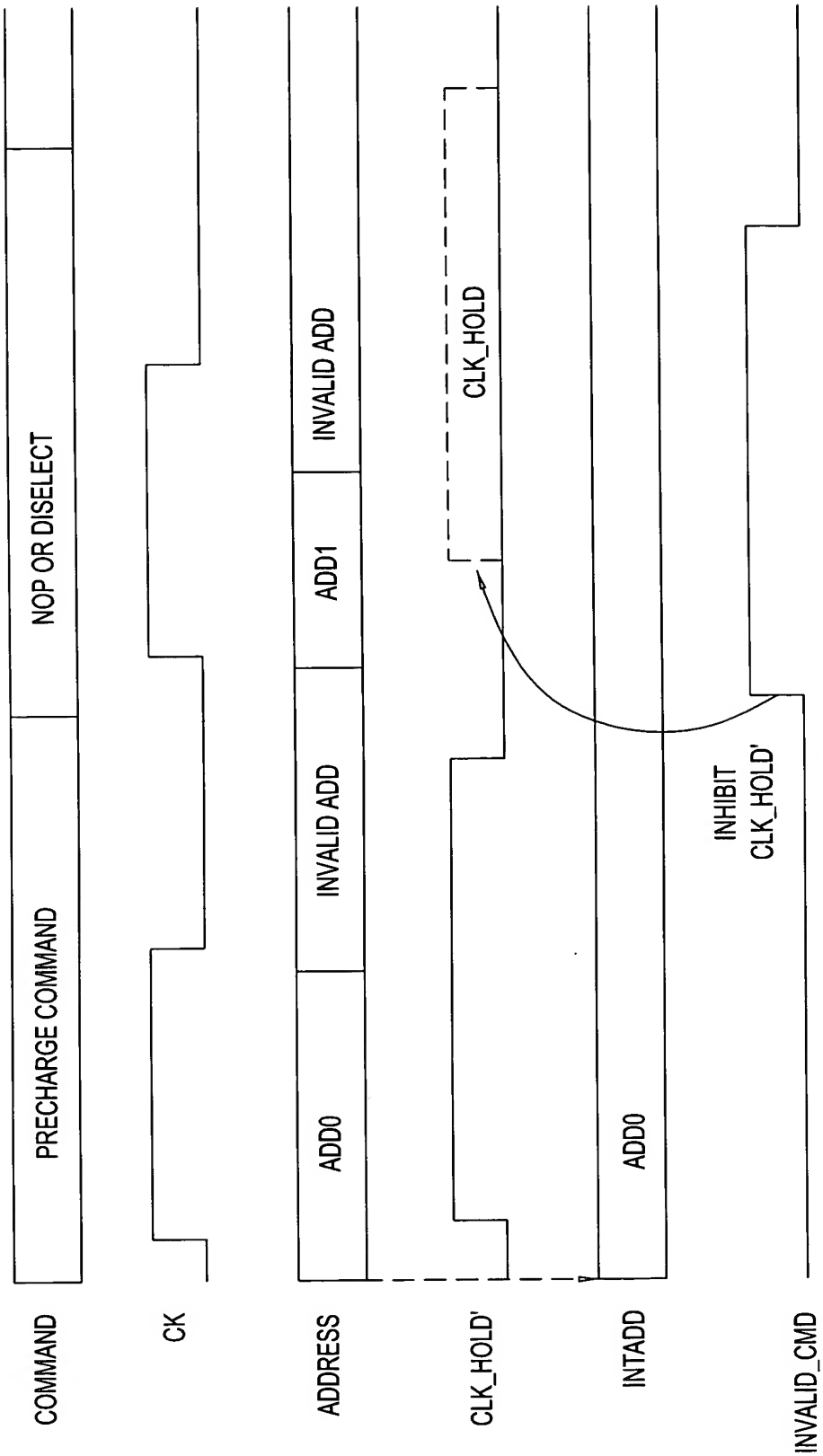
COMMAND
PRECHARGE COMMAND
NOP OR DISELECT
CK
ADDRESS
ADD0
INVALID ADD
ADD1
INVALID ADD
CLK_HOLD'
CLK_HOLD
INTADD
ADD0
INVALID_CMD
INHIBIT
CLK_HOLD'

FIG. 5B

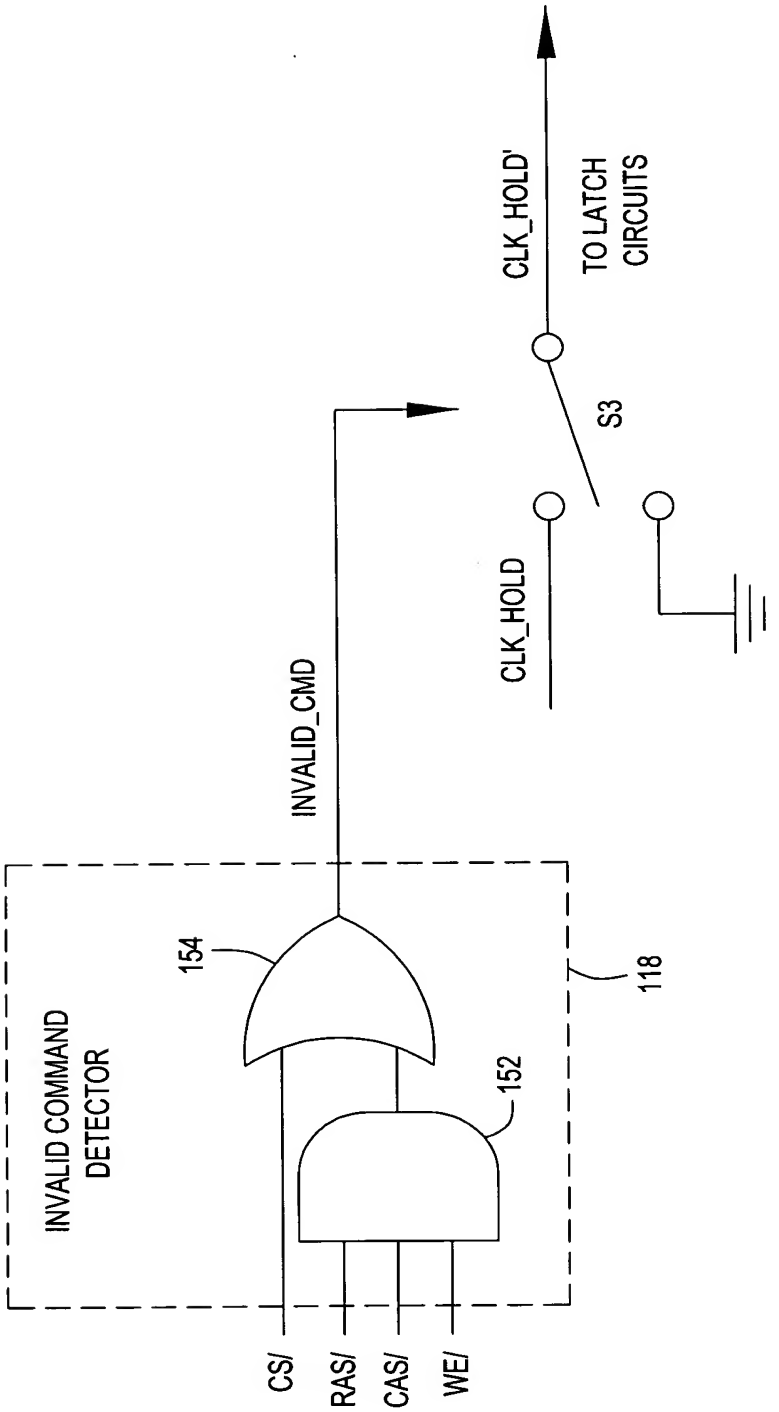
CLK_HOLD'
TO LATCH CIRCUITS
S3
CLK_HOLD
INVALID_CMD
154
152
118
INVALID COMMAND DETECTOR
CS/
RAS/
CAS/
WE/

FIG. 6A

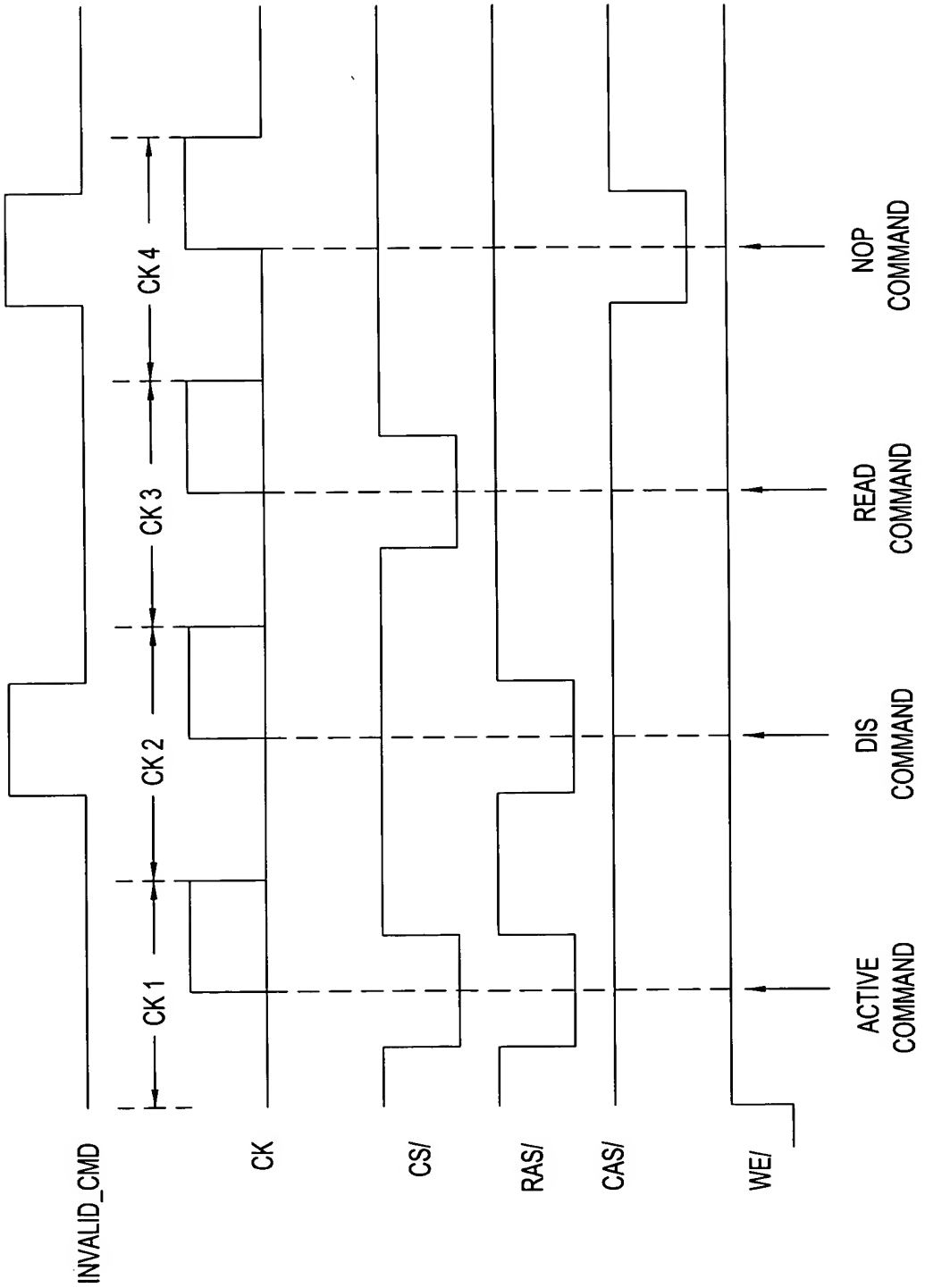
INVALID_CMD
CK
CS/
RAS/
CAS/
WE/
CK 1
CK 2
CK 3
CK 4
ACTIVE COMMAND
DIS COMMAND
READ COMMAND
NOP COMMAND

FIG. 6B